A Comparative Evaluation of SRAM topologies

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***Abstract*— SRAM design at nanotechnology needs to balance area, power consumption, noise tolerance and robust to radiation faults. In this paper the SRAM cells 6T, 8T, 9T and 8T-SER were evaluated. The results showed that 8T and 9T cells obtained the best delay values considering the read of the logical value 1 and the write operation. The 6T cell obtained a good result in the reading of the logical value 0. Evaluating the results of energy, the 8T cell, followed closely by the 9T cell, presented the lowest power consumption. The noise tolerance simulations showed that the 8T-SER SRAM cell, obtained the best results in all noise margins. Analysis for the radiation effects demonstrated that the 8T-SER remained immunity to the effects in half of the cases that were submitted.**

Keywords*— *SRAM, Static Noise Margins, Single Event Upset, CMOS, Robustness.

I. INTRODUCTION

SRAM (Static Random-Access Memory) occupies the largest block area of computer systems, being about 70% of the area of a SoC [1] and about 90% of the area of a processor [2]. These cells must be efficient, robust, consuming low energy and fault tolerance [3]. Decreasing the supply voltage of the SRAMs impacts on the reduction of the noise tolerance, i.e. the reduce the cell ability to maintain the stored value. Moreover, reducing the scaling of the transistors, there is a significant increase in the circuit sensibility for radiation effect [4]. One of the main threats of reliability in nanometric technologies comes from the charged particles that strike with the transistors, causing a deviation in their behavior [4]. This effect on the memory cells is called the SEU (Single Event Upset) [5]. In the past, this effect was limited to radiation-hostile environments. However, with scaling, the SEU effects can also be observed at ground level [4].

Due to all this problem, finding means to effectively balance all these characteristics is essential There are many design techniques to deal with challenges encountered during the development of SRAMs. Many focusing on improving the reliability of operations or sub-threshold voltage regions. However, for the most part these techniques generate gains in some factors, but cause losses in others.

This work evaluates four cells topologies. The electric diagrams of the cells are shown in Fig. 1. The conventional 6T SRAM is the most used in the industry. It has good stability, low consumption and occupies small area [6]. The 8T cell is proposed to operate in ultra-low voltage. This cell occupies a slightly larger area, but has the internal nodes isolated during the read operations [7].9T SRAM cell, based on the 8T cell. With the proposal to improve the performance, dealing with leakage current problems [7]. The 8T-SER is cell proposed to be a SEU robust. The cell has no dedicated access to read operations and is suitable for low voltage and low power applications [8]. This paper aims to evaluate different SRAM cells topologies regarding performance, power, static noise tolerance and robustness to SEU.

II. METHODOLOGY

All analyzes were performed through electrical simulations using the NGSpice tool [9]. The circuits were described using the predictive model of High Performance (HP) in 16nm, provided by Predictive Technology Model (PTM) [10]. These models have the supply voltage in 0.7V. The Table I shows the parameters of the technology, where W stands for the width of the threshold channel, L is the channel length, Tox corresponds to the oxide thickness and Vth0 is the threshold voltage of the long channel device at zero substrate.

In this work, studies were carried out regarding the measurement of operation times, obtaining the energy consumption, the stability analysis for noise and the SEU robustness. All SRAM cells were evaluated considering the same architecture composed for 128 memory cells. This structure is comprised of the Pre-Charge (PRE), the Write Enable (WE) and Sense Amplifier Enable (SAE) circuits. The WE circuit is responsible for adjusting the voltage of the bitlines to perform the write operation. The PRE circuit has the function of maintaining certain voltage in the bitlines during the intervals of operation. The SAE circuit has the objective of measuring the voltage difference between the bitlines, accelerating the read process.

To find out the read and write times, it was necessary to define a sequence of operations that would allow the measurement of this data. In the first step, a write operation of the logic value 0 is performed. After a waiting period (Hold State), a read operation is triggered. The next step is a write the logical value 1. Again, after a hold state, the storage value in the cell is read. This sequence is shortly defined in this paper as write0/read0/write1/read1.

In addition to the sequence of operations, it was necessary to create an auxiliary script to obtain the read and write times, and to measure the power consumption for these operations. The script was implemented in Python language. The writing times were obtained by evaluating the time of 50% the rise voltage of WL (World Line) up to the time of 50% of rise voltage in the node where the logic value 1 will be stored. The reading times were found evaluating the time from 50% of the rise voltage of WL until the time of given voltage difference between bitlines was found. A value of 20mV was set for this difference.

TABLE I. PARAMETERS OF TECHNOLOGY

Parameter		**16nm**
L (nm)		16
W(nm)		32
Tox (nm)		0.95
Vth0 (V)	**NMOS**	0.47965
	PMOS	-0.43121

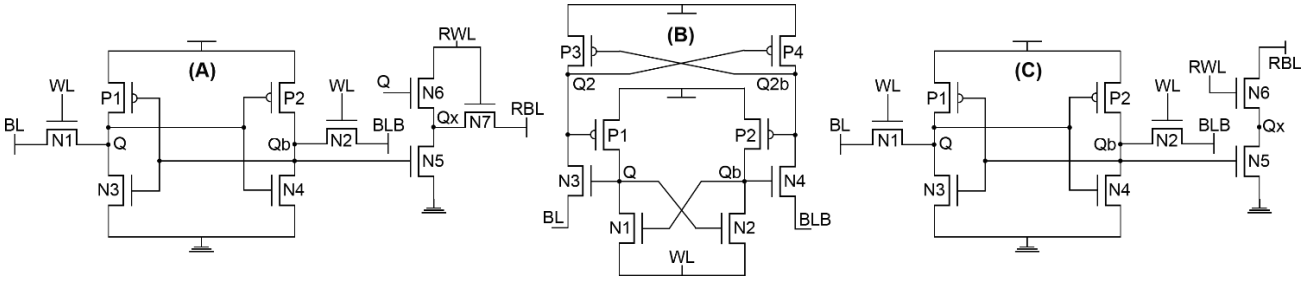

Fig. 1. Diagrams of the cells: (a) 9T SRAM, (b) 8T-SER SRAM and (c) 8T SRAM.

To obtain the energy consumption of each cell, a resource of the electric simulator was used. This feature returns the current consumed by the cell over a period. The interval used was the entire period of the sequence of operations used to obtain the times.

To analyze the noise tolerance of each cell, the method that defines the noise margins as the largest square between the voltage curves was used [11]. These curves correspond to the voltage transfers of the internal nodes of the cells. Fig. 2 illustrate the voltage transfers curves, or butterfly curves. The electric simulator provides the data to form these curves. In Addition, it was necessary to build a script in Python language, dedicated to finding the largest square between these curves.

To evaluate the cells for SEU, we used an analytical model that associates the effects of the collision of the particle with a current source [12]. This model obeyed the behavior of a double exponential, illustrated by Fig. 3. The equation (1) represents the basis of this model, where Qcoll is the collected charge, τα is the time charge constant and τβ is the heavy ion truck time constant [13]. In equation (2) we have the analytic definition of the charge collection, LET (Linear Energy Transfer) being the amount of charge deposited per unit time, while *L* represents the depth of the charge collection, and the constant 10.8fC is the charge that a particle deposit for every 1µm.

$$I(t) = \frac{Qcoll}{\tau\alpha - \tau\beta}\left(e^{-\frac{t}{\tau\alpha}} - e^{-\frac{t}{\tau\beta}}\right) \quad (1)$$

$$Qcoll = 10.8fc\ (L)\ (LET) \quad (2)$$

To perform the SEU simulations another systematic sequence of steps was created. Initially, a write operation is triggered. The cell remains in the Hold state for a period and then a current pulse is injected into one of the sensitive nodes of the cell. The simulation occurs through a new script that applies a binary search to find the smallest current pulse capable of causing a behavior deviation in the cell.

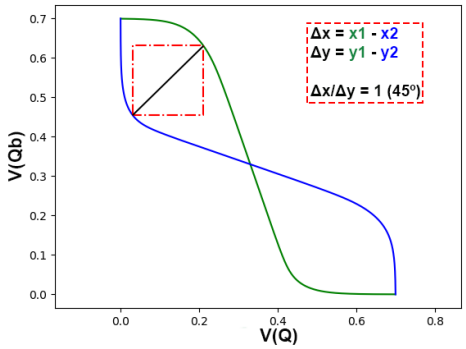

Fig. 2. Butterfly Curve Method.

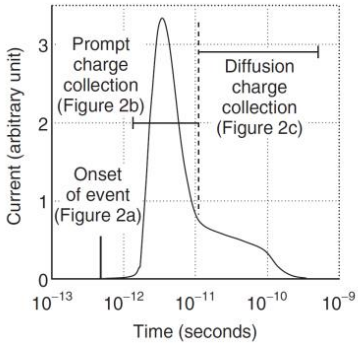

Fig. 3. Mechanisms of Charge Collection [14].

III. Results

In this section the individual results for each cell topology will be presented. These results will be grouped into 4 categories of analysis: Time Evaluation, Energy Consumption, Noise Analysis and SEU Robustness.

A. Time Evaluation

The reading and writing times of the cells considering the worst cases and are available in Table II. Analyzing the performance of the 6T cell in terms of timing, it was observed that the cell requires a longer time to perform the write operation than the read operation. The write operation required about 75% more time than the read. This is due to the greater internal competition during the writing, where the voltage of bitlines must go against the stable arrangement of the inverters. While during reading, there is no guaranteed stability in the bitlines, since the preload circuit is off.

For the 8T cell, a better performance was observed for the write operation in relation to reading. The write operation was about 43% faster than the read operation. This result is possible due to reduced sizing of the pull-down transistors. With this reduction the internal competition during the write operation is reduced. In addition, since this topology uses a dedicated system for reading, this operation is not affected by the reduced sizing of the NMOS transistors.

9T cell present a better result when performing the write operation. The results show a rate of gain being about 56% faster in relation to the read operation. The reason why the results of the 8T and 9T SRAM cells have similar margins, is that both use practically the same concept of layout, differing only in the treatment of leakage current.

It is important to note that both the 8T and 9T cell have immediate response to the read operations of logic value 1. This difference presented earlier between the read and write operations considers the worst case of both cells, that is operations of reading the logic value 0.

For the analysis of the results of the 8T-SER cell a greater time demand was observed to perform the read operation than the write operation. The read was shown to be about 20% slower than the write operation. The write operation occurs more quickly because there is no stability in the voltage of the node that stores the logical value 0. Thus, the internal competition of the cell is reduced, facilitating the writing. Already during the reading operation, the node responsible for storing the logical value 1 must supply its voltage to the bitline, which was pre-charged in ground. However, the transistor responsible for performing this voltage passage is of NMOS type. This impacts on difficulty of raising the bitline voltage, taking more time to perform the read operation.

An important point to be observed was the discrepancy between the values found for this cell relating to the results of the others SRAM cells was large. As already explained in the methodology session, this work applied a similar SRAM structure in all studied memory cells. In order to achieve better performance results for the 8T-SER cell, adjustments could be made. Decrease the cell operation frequency or make changes in the auxiliary circuits are possible solutions that would facilitate the obtaining of the results. However, the objective of this work is to perform a comparison between the cells within the same architecture, so none of these options was adopted.

B. Energy Consumption

The energy results considering a operation sequence of write0/read0/write1/read1 are shown in Table III. The 8T cell had the lowest energy consumption. Similar to 8T, the 9T cell had a slightly higher consumption, about 9%. In addition, the 6T cell showed consuming about 18% more than the 8T cell. Analyzing the 8T-SER it was possible to notice a much higher consumption, surpassing the margin of 1000% higher when compared to 8T cell.

The cells 8T and 9T presented a lower consumption in relation to the 6T cell, even though it had a larger number of transistors. One of the reasons for this result is that the internal NMOS transistors of 8T and 9T cells have a smaller scaling than 6T. Because of this, raising the voltage of the node that storing the logical value 0 occurs more easily. As a result, the PMOS transistor of the reverse node stop to conduct faster. Thus, the critical consumption characterized by the period where the transistors of inverter conduct simultaneously is reduced. In addition, the 8T, and 9T cells have a separate scheme for performing the read operations. This feature avoids the need to connect the internal nodes of the cell to the bitlines during reading. Allowing the node that stores the logic value 1 does not consume energy by maintaining the bitline voltage during the process.

The discrepancy of the energy consumption results of the 8T-SER cell in relation to the others is extreme. However, this is due in large part to the cell characteristic of operating with the pre charge bitlines in ground. Thus, during operations the cell needs to raise the voltage of bitlines. In addition, the transistor responsible for allowing current to pass through the bitlines are of the NMOS type. Impacting on a delay to performing the operation by the characteristic of low conduction of the logical value 1 presented by theses transistors. It is important to note that, different the other cells, the energy cost of pre charge circuit of 8T-SER cell is zero, while in the others cells it is required that the pre charge keep the bitlines constantly charged during the intervals of operation.

C. Noise Analysis

The analysis of data integrity in the presence of noise is shown in Table IV. Considering the robustness for the values found in the SNM (Static Noise Margins), all cells presented an equivalent performance. This is due to the similarity of the analyzed structure. For both cells, analyzing the SNM means subjecting the node to effects of a PMOS and NMOS transistor that can conduct unduly to the noise.

Evaluating the values for RNM (Read Noise Margins) it was verified the greater sensitivity of 6T cell in relation to the other cells. The RNM of the 6T cell was about 72% more sensitive. The reason for the 6T to be more sensitive to RNM is given by the fact of during the reading operation the pass transistors allow the conduction between the bitlines and the internal nodes. Since the bitlines were pre charged, the voltage present in them could aid in the effectiveness of the noise impact. The 8T and 9T cell have a mechanism that perform the read operation in an isolated way of the internal nodes, increasing the robustness for RNM. Already the 8T-SER cell, even allowing the conduction between the bitlines, presented a greater robustness. This is because when the voltage of one of the bitlines begins to rise, the overdrive voltage of the transistor connected with that bitline starts to decrease. Getting to the point where that transistor stops to conduct. Thus, the operation becomes more robust and nondestructive [8].

The results of the WNM (Write Noise Margins) analysis in the cells presented a better performance for the 8T-SER cell, while the other cells obtained similar values. Unlike the read operation, in write the 8T and 9T cells need to connect their internal nodes with the bitlines. In the same way the cell 6T, needs to perform the same process. However, these cells do not present a mechanism similar to that of the 8T-SER cell, already presented in the RNM.

TABLE II. TIME RESULTS

SRAM cell	*Write (ps)*	*Read (ps)*
6T	16	4
8T	8	15
9T	9	16
8T-SER	47	58

TABLE III. ENERGY RESULTS

SRAM Cells	*Energy (fJ)*
6T	0.40
8T	0.34
9T	0.37
8T-SER	4.00

TABLE IV. NOISE RESULTS

SRAM Cells	*SNM (mV)*	*RNM (mV)*	*WNM (mV)*
6T	179	53	281
8T	181	181	292
9T	181	181	292
8T-SER	180	180	363

D. Radiation Robustness

The results obtained for the analysis of the radiation effects, considering SEU effects, showed that for the 1->0 simulations the 8T-SER cell had the best performance, while in the 0->1 the 6T cell was highlighted. The values corresponding to the LET threshold found for each cell are shown in the Table V.

The 6T SRAM cell has a smaller number of nodes susceptible to SEU. But all nodes were affected at some point in the simulation. The 8T and 9T cells have an extra node. In relation to 6T, due to their dedicated reading scheme. However, this node proved to be robust to the effects of a particle collision. This occurs because the node is isolated from the internal structure of the cell, not affecting the value stored by cell. Even so, their internal nodes proved more sensitive compared to 6T cell. The 8T-SER has the highest number of sensitive nodes, being twice as many nodes as the 6T. However, this cell presented total immunity to the radiation effects in 50% of the simulations to which it was submitted. The cell was built with a focus on the robustness, because of that its nodes are punctually isolated depending on the value that the cell is storing. Both 6T, 8T and 9T will present more sensibility for the 1->0 simulations. As the 8T-SER cell was more sensitive in 0->1 simulation.

TABLE V. LET THRESHOLD EVALUATION

SRAM Cells	***LET (KeVcm²/mg)***	
	0->1	***1->0***
6T	255.1	96.8
8T	175.9	87.9
9T	184.7	96.7
8T-SER	149.5	193.5

IV. CONCLUSION

This work demonstrated the impact of reduction in technological node on SRAM cells. The circuits described in a 16nm obtained gains of performance and energy consumption. However considerable losses of robustness and stability. In addition, smaller technological nodes allow a considerable gain in occupied area.

Individual cell analysis showed that the 6T cell obtained the best reading delay. However, the results of RNM showed low stability during the read operation. The 8T cell obtained better delay for writing and loss in reading performance compared to 6T. However, this is compensated by high stability demonstrated by noise analysis. In addition, the cell has a lower energy consumption than the 6T cell. With results similar to those of 8T, the 9T cell has presented good delay times and internal stability, losing in relation to the energy consumption and the occupied area compared to 8T. The 8T-SER cell is not a proposal focused on performance, but on stability and robustness. The cell presented values equivalent to 8T and 9T for SNM and RNM, but with a significant gain in WNM.

For the SEU evaluation, the 8T-SER was more robust than the other cells, taking into account the worst cases. Mainly due to the greater robustness in the simulations 1->0. Even so, you will not be able to achieve an equivalent rate of gain shown in original proposal at 65nm.

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